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comments and bulletins
concerning your
COMMODORE PET

The Transactor

BULLETIN #3
July 31, 1978

MORE INFORMATION REGARDING PET AND ITS PERIPHERALS

1. The PET 2001 now has CSA approval and deliveries from late August onwards will be CSA built PET.
2. Deliveries of the PET printer are not expected until late September due to a revised housing.
3. Second cassettes are now available in Canada and being shipped to Commodore dealers.
4. Floppy disc drive will be available from Commodore November/December.
5. Expansion memory - details of this will be announced in the next bulletin.

Enclosed with this bulletin are two extremely useful releases.

1. A Description of the IEEE-488 BUS for the PET.
2. Pet Interfaces and Lines to the Outside World.

In the next bulletin, we will issue a comprehensive release on operations with the PET through the various peripherals including the built-in cassette.

Any CPU Club member wishing to pass information to other members may do so by writing to CPU Club care of Commodore Business Machines Limited, 3370 Pharmacy Avenue, Agincourt, Ontario, M1W 2K4.

Encs.

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PET INTERFACES AND LINES TO THE OUTSIDE WORLD

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1.

INTRODUCTION

This supplement contains general background information on the PET interfaces and lines to the 'outside world'.

This information is relevant to users who wish to interface with any device external to the PET computer itself. The device could be a printer; a source of digital data such as a seismograph or other scientific instrument; a second cassette tape deck, or an extra memory to increase the power of the PET still further.

This document is intended to provide essential information for the experienced user, who is anxious to explore the interface possibilities of the PET.

2.

CONNECTOR ORIENTATION

As indicated in Figure 2-1, there are four connectors provided, accessible through slots in the rear and side of the PET that enable the user to interface the computer with external devices.

As outlined in Figure 2-2 edge card connectors are utilized, that are in fact direct extensions of the PET main logic assembly board itself. There are two contacts to each position of the connector. The contact identification convention for J1 and J2 is also illustrated in Figure 2-2.

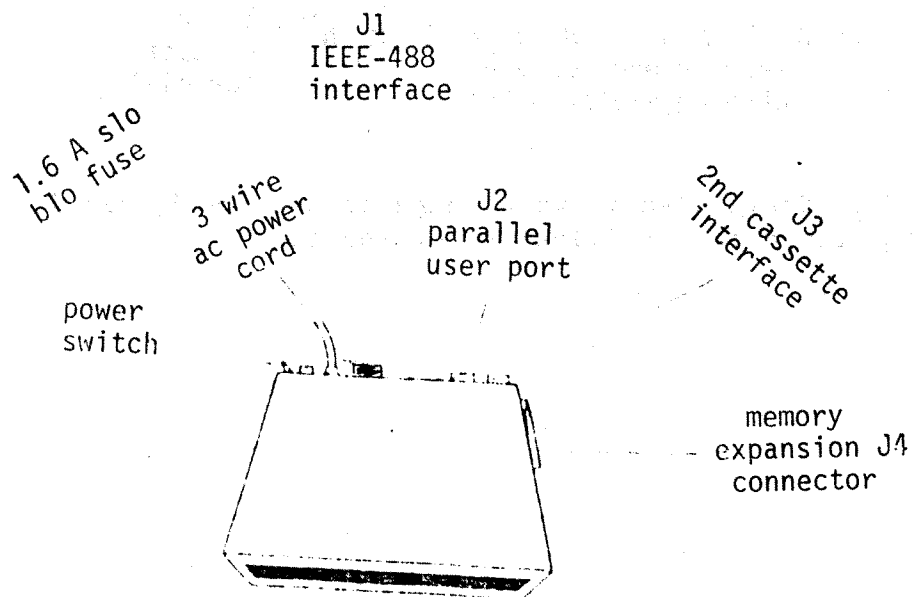


Figure 2-1. Simplified top view of PET showing switch, fuse, line cord and interfacing connectors.

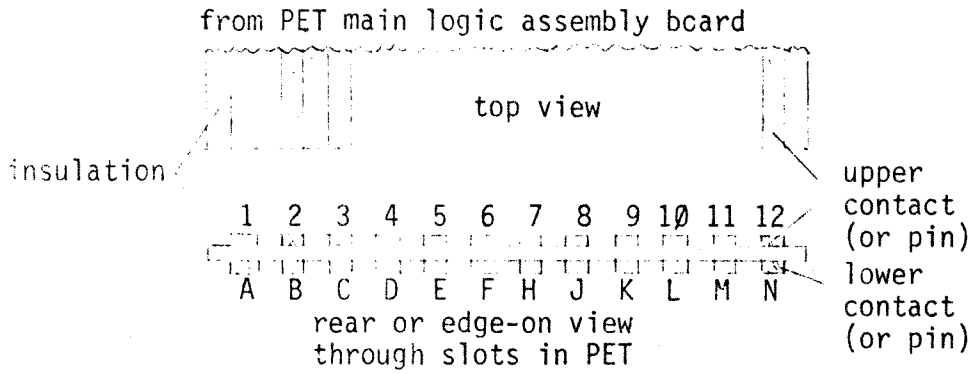


Figure 2-2. Simplified views of edge connectors J1 and J2 to illustrate contact identification convention.

3. IEEE-488 INTERFACE (Connector J1).

The standard IEEE-488 connector is not used on the PET. Instead, a standard 12 position 24 contact edge connector with .156 inch spacing between contact centers is provided. This permits it to be compatible with all of the other connections to the PET.

Keying slots are located between pins 2-3 and 9-10.

Table 3-1 shows the PET contact identification characters; the connection for a standard IEEE connector; the IEEE mnemonics and the signal definitions.

Electrical drive capability and line impedance matching is in accordance with IEEE-488 specifications.

	PET PIN CHARACTERS	STANDARD IEEE CONNECTOR PIN NUMBERS	IEEE SIGNAL MNEMONIC	SIGNAL DEFINITION/LABEL
UPPER PINS	1	1	DI01	Data input/output line # 1
	2	2	DI02	2
	3	3	DI03	3
	4	4	DI04	4
	5	5	EOI	End or identify
	6	6	DAV	Data valid
	7	7	NRFD	Not ready for data
	8	8	NDAC	Data not accepted
	9	9	IFC	Interface clear
	10	10	SRQ	Service request
	11	11	ATN	Attention
	12	12	GND	Chassis ground and IEEE cable shield drain wire
LOWER PINS	A	13	DI05	Data input/output line # 5
	B	14	DI06	6
	C	15	DI07	7
	D	16	DI08	8
	E	17	REN	Remote enable
	F	18	GND	DAV ground
	H	19	"	NRFD ground
	J	20	"	NDAC ground
	K	21	"	IFC ground
	L	22	"	SRQ ground
	M	23	"	ATN ground
	N	24	"	Dataground (DI01-8)

Table 3-1. PET contact identification characters. IEEE-488 identification characters, associated labels and descriptions.

3.1

RECEPTACLES FOR THE IEEE INTERFACE

A list of frequently used 12 position 24 contact receptacles that are suitable for connection to the PET edge card connector J1 and J2 is shown in Table 3-2.

MANUFACTURER	PART NUMBER
Cinch	251-12-90-160
Sylvania	6AG01-12-1A1-01
Amp	530657-3
Amp	530658-3
Amp	530654-3

Table 3-2. Receptacles recommended for PET IEEE-488 connectors or parallel user port.

3.2

IEEE-488 CONNECTORS

The IEEE-488 standard receptacles are not directly connectable to the PET edge connector; some of these are shown in Table 3-3, and belong to the Cinch Series 57 or Champ Series (Amphenol). Also shown are their matching plugs.

CONNECTOR MANUFACTURER	IDENTIFIER	DESCRIPTION
Cinch	5710240	Solder-plug.
"	5720240	Solder-receptacle.
AMP	552301-1	Insulation displacement plug.
"	552305-1	Insulation displacement receptacle.

Table 3-3. IEEE standard connectors not suitable for PET.

Commodore has available a 1 meter long IEEE-488 dual connector-PET edge connector, cable. Please contact your local dealer, or Commodore, for price and delivery.

4.

PARALLEL USER PORT (Connector J2).

The lines for this interface are brought out from the PET main logic board to a 12 position, 24 contact edge connector with .156 inch spacing between contact centers. See Table 3-2 for suitable mating connectors.

Keying slots are located between pins 1-2 and 10-11.

Table 4-1 shows the PET pin identification characters, the corresponding labels and their descriptions.

Note that the connections 1-12, that is the top line of contacts (see figure 2-2) are primarily intended for use by the PET service department or qualified dealers. When using the incorporated ROM diagnostic, a special connector is used; this jumpers some of the top contacts to the bottom contacts. It is strongly advised that the top connectors 1-12 be used only with extreme caution.

PIN IDENTIFICATION CHARACTER	SIGNAL LABEL	SIGNAL DESCRIPTION
1	Ground	Digital ground.
2	T.V. Video	Video output used for external display, used in diagnostic routine for verifying the video circuit to the display board.
3	IEEE SRQ	Direct connection to the SRQ signal on the IEEE-488 port. It is used in verifying operation of the SRQ in the diagnostic routine.
4	IEEE EOI	Direct connection to the EOI signal on the IEEE-488 port. It is used in verifying operation of the EOI in the diagnostic routine.
5	Diagnostic Sense	When this pin is held low during power up the PET software jumps to the diagnostic routine, rather than the BASIC routine.
6	Tape #1 READ	Used with the diagnostic routine to verify cassette tape #1 read function.
7	Tape #2 READ	Used with the diagnostic routine to verify cassette tape #2 read function.
8	Tape Write	Used with the diagnostic routine to verify operation of the WRITE function of both cassette ports.
9	T.V. Vertical	T.V. vertical sync signal verified in diagnostic. May be used for external TV display.
10	T.V. Horizontal	T.V. horizontal signal verified in diagnostic may be used for TV display.
11, 12	GND	Digital ground

Table 4-1. Parallel user port information. PET pin identification characters, the corresponding signal labels and their descriptions.

PIN IDENTIFICATION CHARACTERS	SIGNAL LABEL	SIGNAL DESCRIPTION
A	GND	Digital ground.
B	CA1	Standard edge sensitive input of 6522 VIA.
C	PA 0	Input/output lines to peripherals, and can be programmed independently of each other for input or output.
D	PA1	"
E	PA2	"
F	PA3	"
H	PA4	"
J	PA5	"
K	PA6	"
L	PA7	"
M	CB2	Special I/O pin of VIA.
N	GND	Digital ground.

Table 4-1 (continued). Parallel user port information. PET pin identification characters, the corresponding signal labels and their descriptions.

4.1 VERSATILE INTERFACE ADAPTER

The lines on the bottom side of the user port connector originate from a Versatile Interface Adapter (VIA MOS Technology part # 6522).

The signals CA1, PA0-7 and CB2, are directly connected to a standard 6522 VIA located at hexadecimal address E840. (Decimal address 59456).

The parallel port consists of eight programmable bi-directional I/O lines PA0-7, an input handshake line for the eight lines, CA1 which can also be used for other edge sensitive inputs and a very powerful connection CB2. This has most of the abilities of CA1, but can also act as the input or output of the VIA shift register.

A detailed specification for the VIA is attached. All signals on the VIA that are not connected to the user port are utilized by the PET for internal controls. Please note that the user should avoid interfacing with these signals in any way.

Table 4-2 shows the decimal and hexadecimal addresses in the PET associated with the VIA.

DECIMAL	HEXADECIMAL	\$E840+	ADDRESSED LOCATION
59456	E840	0000	Output register for I/O port B.
59457	E841	0001	Output register for I/O port A with handshaking.
59458	E842	0010	I/O Port B Data Direction register.
59459	E843	0011	I/O Port A Data Direction register.
59460	E844	0100	Read Timer 1 Counter low order byte Write to Timer 1 Latch low order byte.
59461	E845	0101	Read Timer 1 Counter high order byte. Write to Timer 1 Latch high order byte and initiate count.
59462	E846	0110	Access Timer 1 Latch low order byte.
59463	E847	0111	Access Timer 1 Latch high order byte.
59464	E848	1000	Read low order byte of Timer 2 and reset Counter interrupt Write to low order byte of Timer 2 but do not reset interrupt.
59465	E849	1001	Access high order byte of Timer 2; reset Counter interrupt on write.
59466	E84A	1010	Serial I/O Shift register.
59467	E84B	1011	Auxiliary Control register.
59468	E84C	1100	Peripheral Control register.
59469	E84D	1101	Interrupt Flag register (IFR).
59470	E84E	1110	Interrupt Enable register.
59471	E84F	1111	Output register for I/O Port A, without handshaking.

Table 4-2. VIA 6522 Decimal and Hexadecimal addresses in PET.

4.2 PROGRAMMING THE USER PORT

Data lines PA0-7 are individually programmed to function for input or output as required. This is done by using a software POKE 59459 command to place a number into the data direction register. This number must contain zeros on bits corresponding to lines where inputs are required and ones where outputs are required. Table 4-3 shows a practical example of input/output selection.

The programming need only be carried out at the beginning. From then on POKE 59471 can be used to drive the pins programmed as outputs, and PEEK 59471 will read all the inputs.

COMMAND STATEMENT	BINARY REPRESENTATION	LINES	MODE
POKE 59459,255	11111111	PA0-7	Output
POKE 59459,0	00000000	PA0-7	Input
POKE 59459,240	11110000	PA0-3 PA4-7	Input Output

Table 4-3. Parallel user port example. Programming of lines PA0-7 for input/output operation.

5. SECOND CASSETTE INTERFACE (Connector J3).

This interface is brought out from the PET main logic board to a 6 position 12 contact edge connector with .156 inch spacing between contact centers (see Figure 5-1).

A keying slot is located between pins 2-3.

This port is intended for use with the Commodore second cassette system only. Any other connections are made at the risk of the user. Please note that the +5 volts is not intended for use as an external power supply.

Table 5-1 shows the PET pin identification characters, labels and descriptions. Table 5-2 shows some typical receptacles that are suitable for the second cassette connector.

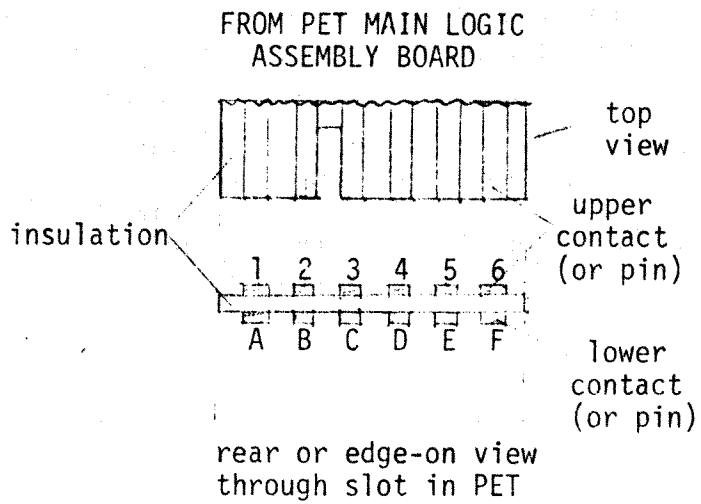


Figure 5-1. Simplified view of edge connector J3 with contact identification.

PIN IDENTIFICATION CHARACTERS	LABEL	DESCRIPTION
A-1	GND	Digital ground.
B-2	+5	Positive 5 volts to operate cassette circuitry only.
C-3	Motor	Computer controlled positive 6.volts for cassette motor.
D-4	Read	Read line from cassette.
E-5	Write	Write line to cassette.
F-6	Sense	Monitors closure of mechanical switch on cassette when any button is pressed.

Table 5-1. Second cassette interface port. PET pin identification characters, labels and associated descriptions. Note A-1, B-2, etc implies a pin A to pin 1, pin B to pin 2, connection. In some special machines, pins 1 through 6 were not connected.

MANUFACTURER	IDENTIFIER
Sylvania	6AJ07-6-1A1-01
Viking	2KH6/1AB5
Viking	2KH6/9AB5
Viking	2KH6/21AB5
Amp	530692-1
Sullins	ESM6-SREH
Cinch	250-06-90-170

Table 5-2. A selection of suitable receptacles for connecting with the PET second cassette edge connector J3.

6. MEMORY EXPANSION CONNECTOR (Connector J4).

The memory expansion connector provides access to the buffered and decoded input/output lines from the 6502 microprocessor. Figure 6-1 shows a simplified view of the 40 position - 80 contact edge connector used. The spacing between contact centers is 0.1 inch.

Note that the 40 top edge 'B' connections (or pins) are ground returns for the corresponding 40 lower edge 'A' connections.

Table 6-1 shows the PET pin numbers, line labels and line descriptions.

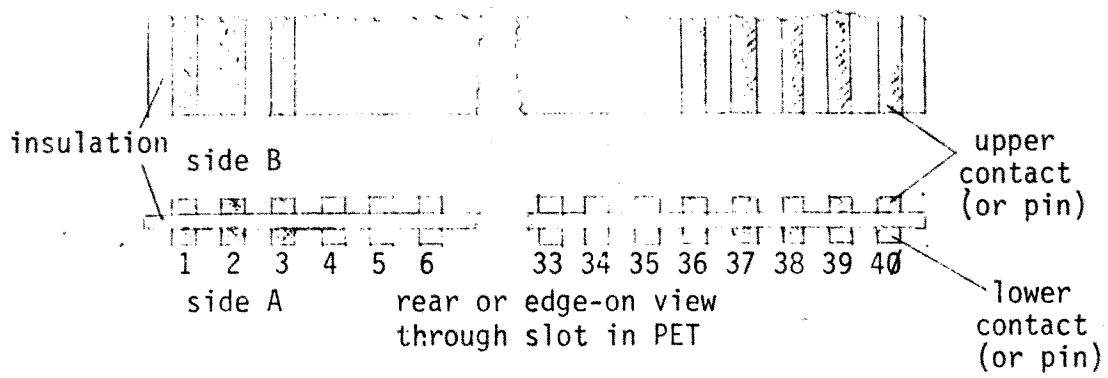


Figure 6-1. Simplified view of edge connector J4 with contact identification. All side B contacts grounded.

SIDE A PIN NUMBERS	LINE LABELS	LINE DESCRIPTION
A1	BA0	Address bit 0, used for memory expansion. Buffered.
A2	BA1	Address bit 1, used for memory expansion. Buffered.
A3	BA2	Address bit 2, used for memory expansion. Buffered.
A4	BA3	Address bit 3, used for memory expansion. Buffered.
A5	BA4	Address bit 4, used for memory expansion. Buffered.
A6	BA5	Address bit 5, used for memory expansion. Buffered.
A7	BA6	Address bit 6, used for memory expansion. Buffered.
A8	BA7	Address bit 7, used for memory expansion. Buffered.
A9	BA8	Address bit 8, used for memory expansion. Buffered.
A10	BA9	Address bit 9, used for memory expansion. Buffered.
A11	BA10	Address bit 10, used for memory expansion. Buffered.
A12	BA11	Address bit 11, used for memory expansion. Buffered.
A13	NC	No connection.
A14	NC	No connection.
A15	NC	No connection.
A16	<u>SEL 1</u>	4K byte page address select for memory locations 1000-1FFF.
A17	<u>SEL 2</u>	4K byte page address select for memory locations 2000-2FFF.

Table 6-1. Memory expansion connector. PET pin numbers. Line labels and line descriptions.

Table 6-1 (continued)

SIDE A PIN NUMBERS	LINE LABELS	LINE DESCRIPTION
A18	$\overline{\text{SEL 3}}$	4K byte page address select for memory locations 3000-3FFF.
A19	$\overline{\text{SEL 4}}$	4K byte page address select for memory locations 4000-4FFF.
A20	$\overline{\text{SEL 5}}$	4K byte page address select for memory locations 5000-5FFF.
A21	$\overline{\text{SEL 6}}$	4K byte page address select for memory locations 6000-6FFF.
A22	$\overline{\text{SEL 7}}$	4K byte page address select for memory locations 7000-7FFF.
A23	$\overline{\text{SEL 9}}$	4K byte page address select for memory locations 9000-9FFF.
A24	$\overline{\text{SEL A}}$	4K byte page address select for memory locations A000-AFFF.
A25	$\overline{\text{SEL B}}$	4K byte page address select for memory locations B000-BFFF.
A26	NC	No connection.
A27	$\overline{\text{RES}}$	Reset for 6502 microprocessor. Note: Connected to 74LS00 output.
A28	$\overline{\text{TRQ}}$	Interrupt request line to the micro-processor.
A29	B02	Buffered phase 2 clock.
A30	R/W	Buffered read/write from 6502 micro-processor.
A31	NC	No connection.
A32	NC	No connection.
A33	BD0	Data bit 0. Buffered
A34	BD1	Data bit 1. Buffered
A35	BD2	Data bit 2. Buffered
A36	BD3	Data bit 3. Buffered
A37	BD4	Data bit 4. Buffered
A38	BD5	Data bit 5. Buffered
A39	BD6	Data bit 6. Buffered
A40	BD7	Data bit 7. Buffered

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A SHORT DESCRIPTION OF THE IEEE-488 BUS FOR THE PET

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 - 1.3.2 PET/IEEE Bus Timing Constraints
 - 1.4 The Management Bus
2. IEEE Signals and Definitions
 - 2.1 Logic Level Convention
3. Status Word (ST)
4. IEEE-488 Register Addresses

1. INTRODUCTION TO THE IEEE-488 BUS

This bus consists essentially of 16 signal lines that are divided functionally into three groups, there are:

- (1) The data transmission bus
- (2) The control bus
- (3) The management bus

Furthermore, the IEEE bus can support three classes of device:

- (1) Talkers: at any given moment, only one device is permitted to transmit data to the data bus.
- (2) Listeners: as many devices as required may receive data simultaneously from the bus.
- (3) Controller: the PET is the only controller allowed on the IEEE bus.

The function and mode of operation of the data, control and management busses are discussed in Sections 1.2 through 1.4.

1.1 BUS/DEVICE CONNECTION

The line-pin connections for the 12 position 24 contact edge card connector emanate from the PET main assembly board (see Table 1-1). For further information, please refer to Figure 2-2 in 'PET Interfaces and Lines to the Outside World'.

Certain physical limitations should be noted when connecting devices to the IEEE bus:

- (1) The maximum advisable bus extension from the PET is 20 meters.
- (2) The maximum interdevice spacing is 5 meters.
- (3) The maximum number of devices is 15.

PET CONTACT IDENTIFICATION	BUS	IEEE LABEL	IEEE CONTACT IDENTIFICATION	LABEL DESCRIPTION
1 2 3 4	DATA	DI01 DI02 DI03 DI04	1 2 3 4	Data INPUT/OUTPUT LINE #1 Data INPUT/OUTPUT LINE #2 Data INPUT/OUTPUT LINE #3 Data INPUT/OUTPUT LINE #4
5	MANAGER	EOI	5	End or identify.
6 7 8	TRANSFER	DAV NFRD NDAC	6 7 8	Data valid. Not ready for data. Data not accepted.
9 10 11 12	MANAGER	IFC SRQ ATN SHIELD	9 10 11 12	Interface clear. Same as PET reset. Service request. Attention. Chassis ground and IEEE cable shield.
A B C D	DATA	DI05 DI06 DI07 DI08	13 14 15 16	Data INPUT/OUTPUT LINE #5 Data INPUT/OUTPUT LINE #6 Data INPUT/OUTPUT LINE #7 Data INPUT/OUTPUT LINE #8
E	MANAGER	REN	17	Remote enable (REN) always ground in the PET.
F H J K L M N	GROUNDS	GND6 GND7 GND8 GND9 GND10 GND11 LOGIC GND	18 19 20 21 22 23 24	DAV ground NFRD ground NDAC ground IFC ground SRQ ground ATN ground Data ground (DI01-8)

Table 1-1. IEEE bus group, label and contact identification number.

1.2 THE DATA BUS

This bus is comprised of 8 bi-directional lines that transmit the active low data signals DI01-8. The slowest device in use on the bus at a given time controls the rate of data transfer; the mode of transfer is one byte at a time, bit-parallel.

Peripheral addresses and control information are also transmitted on the data bus. They are differentiated from data by ATN (true) during their transfer.

The most significant bit (MSB) is on line DI08.

For an explanation of signal abbreviations such as DI01-8, see Section 2.

1.2.1 DATA TRANSMISSION MODES

All possible bit patterns are valid on the data bus when sending data to devices.

1.3 THE TRANSFER BUS

This three line bus controls the transfer of data over the data bus. The signals transmitted are used in the handshake procedure outlined in Section 1.3.1.

These signals are:

- | | | |
|-----|------|---------------------|
| (1) | NRFD | Not ready for data. |
| (2) | NDAC | Data not accepted. |
| (3) | DAV | Data valid. |

Note that the talker originates the DAV signal and the listeners the NRFD and NDAC signals.

See Table 2-1 for detailed description of signals.

1.3.1 THE HANDSHAKE PROCEDURE

When a talker transmits a data byte to one or more listeners, this control procedure is used in order to ensure that the operation is successful.

The essential function of the handshake is to ensure:

- (1) All listeners are ready to accept data.
- (2) That there is valid data on the data bus.
- (3) That the data has been accepted by all listeners.

The transfer of data occurs at a rate determined by the slowest active device on the bus; this allows the interconnection of devices which handle data at different speeds.

The sequence of events that occur during the transfer of a data byte from the talker to the listeners is shown in the flow diagram of Figure 1-1.

Figure 1-2 shows the relative timing of transfer bus signals during a typical handshake; the bracketed numbers in the following sequence refer to the changes in signal logic levels in the Figure:

- (1) NRFD goes high (false) indicating that all listeners ready for the next byte of data.
- (2) The talker puts the next data byte on the data bus and allows the data signals to settle. This could happen before, after or during (1).
- (3) The talker tests NRFD, when it is found to be high the talker makes DAV low (true) to inform listeners that the bus data is now valid.
- (4) As soon as a single listener detects that DAV is low that listener sets NRFD low; data is now accepted by all the individual listeners at their own rate, each of whom release NDAC as they accept the data.
- (5) NDAC goes high (false) when the slowest of the listeners have accepted the data.
- (6) The talker sets DAV high (false) indicating that the data bus signals are now invalid.
- (7) The listeners note that DAV has gone high and sets NDAC low (true) completing the hand shake. When each listener has processed the data they release NRFD. This terminates the sequence for the first data transfer. The sequence will repeat again beginning at (1) until all required data transfers have been completed.

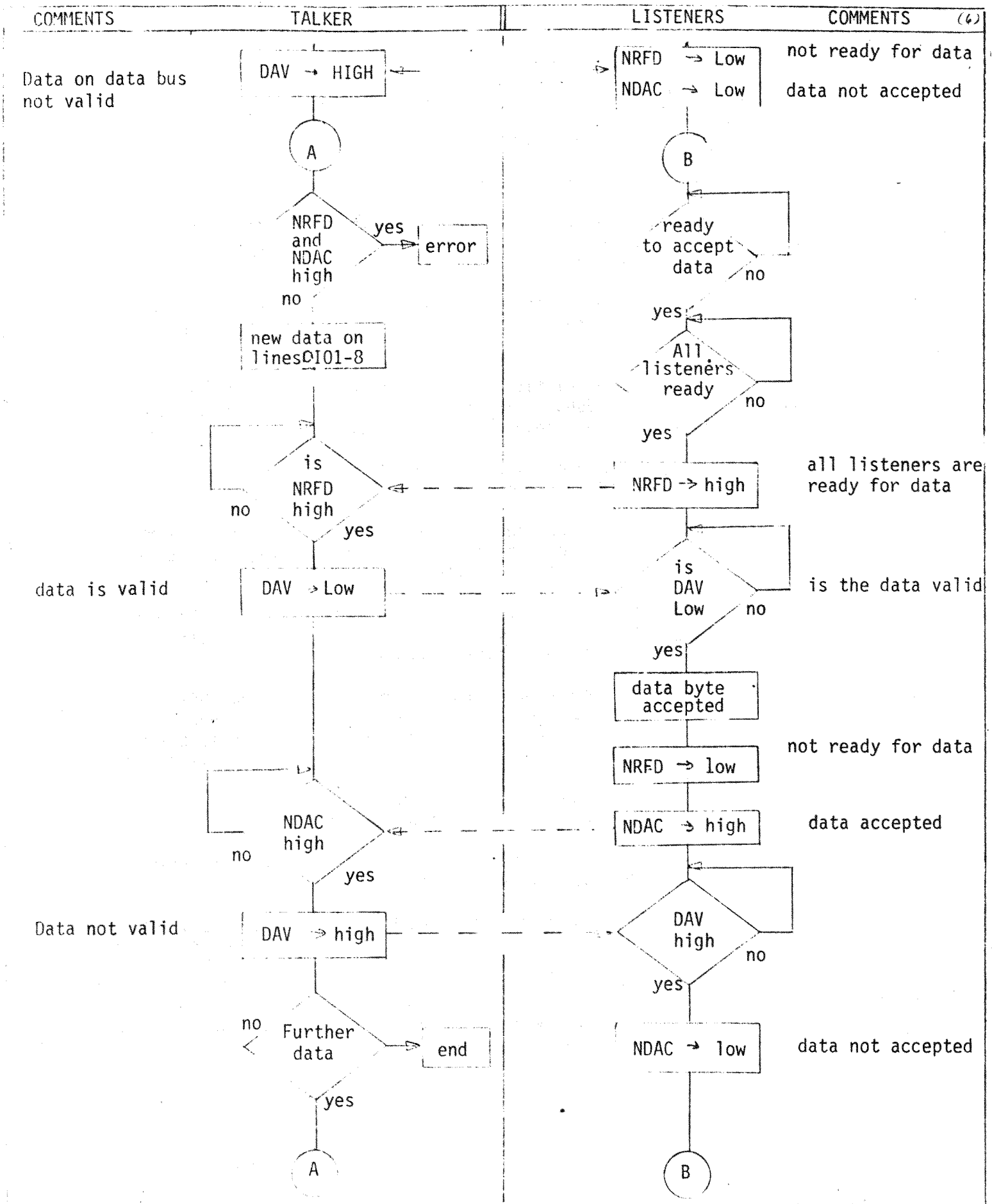


Figure 1-2. Sequence of events during a data byte transfer from the talker to the listeners. Broken lines indicate the testing of transfer bus signal logic levels.

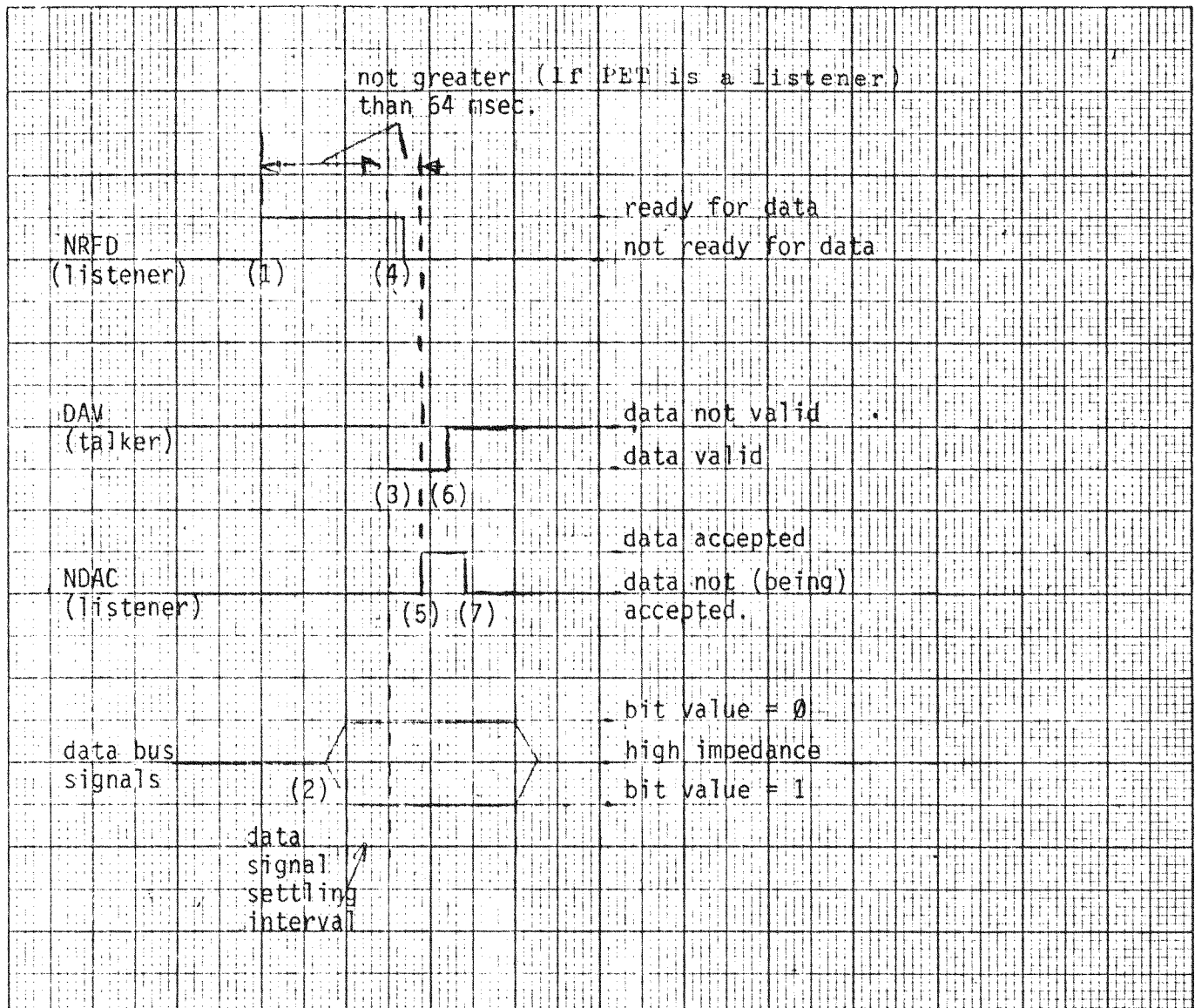


Figure 1-1. Transfer bus handshake sequence. Numbers (1) - (7) refer to Section 1.3.1.

1.3.2 PET/IEEE BUS TIMING CONSTRAINTS

The following limitations should be noted in order to avoid a loss of data:

- (1) When PET is a listener, it expects DAV to go low within 64 milliseconds after it has set NRFD high.
- (2) When PET is a talker, it expects NDAC to go high within 64 milliseconds after it has set DAV low.

If these limitations are exceeded, the PET ceases to transfer and sets the appropriate status word (ST). See Table 3-1.

1.4 THE MANAGEMENT BUS

This group of five signal lines controls the state of the data bus and defines its signals; these can be concerned with data, addresses, or control information (device commands).

The five management signals are:

- | | | | |
|-----|-----|-----------------|--|
| (1) | ATN | Attention. | Assigns devices to act as listeners or talkers. |
| (2) | EOI | End or identify | Indicates that last data byte is being transferred |
| (3) | IFC | Interface clear | Initializes the data bus. Talkers and listeners set idle. Same signal as reset in the PET. |
| (4) | SRQ | Service request | Device tells controller that service is required. Not implemented in BASIC but available in PET. |
| (5) | REN | Remote enable | Permanently tied to ground in the PET. |

2. IEEE-488 SIGNALS AND DEFINITIONS

The 16 transmission lines of the IEEE-488 bus are each assigned a specific signal. Table 2-1 gives the bus group, name, abbreviation and functional description for each of these signals.

2.1

LOGIC LEVEL CONVERSION

The 'true' or logical "1" is low with common collector type outputs. This allows any device to hold the bus in the 'true' or logical "1" state.

BUS GROUP	SIGNAL ABBREV.	NAME	FUNCTIONAL DESCRIPTION
Manager	ATN	Attention	The PET (controller) sets this signal low while it is sending commands on the data bus. When ATN is low, only peripheral addresses and control messages are on the data bus. When ATN is high, only previously assigned devices can transfer data.
Transfer	DAV	Data Valid	When DAV is low, this signifies that data is valid on data bus.
Manager	EOI	End or Identify	When the last byte of data is being transferred, the talker has the option of setting EOI low. The PET always sets EOI low while the last data byte is being transferred from the PET.
Manager	IFC	Interface clear	The PET sends its internal reset signal as IFC low (true) to initialize all devices to the idle state. When PET is switched on or reset, IFC goes low for about 100 milliseconds.
Transfer	NDAC	Data not accepted	This signal is held low (true) by the listener while reading. When the data byte has been read, the listener sets NDAC high. This signals the talker that data has been accepted.
Transfer	NRFD	Not ready for data	When NRFD is low (true), one or more listeners are not ready for the <u>next</u> byte of data. When all devices are ready, NRFD goes high.
Manager	SRQ	Service request	Not implemented in BASIC, but available to the PET user.
Manager	REN	Remote enable	REN is held low by the bus controller. The PET has a pin grounded that keeps REN permanently low.

Table 2-1 IEEE-488 bus signal.

BUS GROUP	SIGNAL ABBREV.	NAME	FUNCTIONAL DESCRIPTION
Data	DIO1-8	Data input/output lines 1 through 8	These signals represent the bits of information on the data bus. When a DIO signal is low, it represents 1 and when high 0.
General	GND	Ground	Ground connections: There are six control and management signal ground returns, one data signal ground return and one chassis shield ground lead.

Table 2-1 (continued)

3. STATUS WORD (ST)

ST is a BASIC variable which can be used to check the outcome of INPUT/OUTPUT operations. ST can have certain values over the range 0-128. Table 1-4 shows the status code that appertains to the IEEE-488 bus.

ST	ERROR	EXPLANATION
1	Time out on listener	The IEEE device has not responded within the 65 milliseconds time out interval.
2	Time out on talker	The IEEE device has <u>not</u> provided an active 'data valid' signal (DAV low) within the 65 millisecond time out interval.
64	End or identify (EOI)	EOI has gone low (true), on the last byte of data being transferred on IEEE bus. Note that all devices do not generate an EOI signal. Consult relevant instrument manual.
-128	Device not present	Device did not respond when addressed; this generates an error message and the operating system returns the PET to BASIC command level.

Table 3-1. ST status code for IEEE-488 bus.

4. IEEE-488 REGISTER ADDRESSES

Table 4-1 shows the IEEE-488 hardware addresses for the PET. An attempt to control the bus by means of the PEEK and POKE commands will fail, if the time out intervals for the 488 devices are exceeded.

HEX ADDRESS	DECIMAL ADDRESS	BITS	IEEE	MODE
E820	59424	0-7	DI01-8	Input
E822	59426	0-7	DI01-8	Output
E821	59425	3	NDAC	Output
E823	59427	3 4	DAV SRQ	Input
E810	59408	6	EOI	Input
E840	59456	0 1 2 6 7	NDAC NRFD ATN NRFD DAV	Input Output Output Input Output

Table 4-1. IEEE-488 hardware addresses and signal information.

Appended is a table that gives code assignments for the command mode of operation on the IEEE bus.

Table 2. Code Assignments for "Command Mode" of Operation.

(SENT AND RECEIVED WITH ATN TRUE)

Bits		b ₄	b ₃	b ₂	b ₁	MSG		MSG		MSG		MSG		MSG		MSG		MSG	
b ₇ b ₆ b ₅		b ₄ b ₃		b ₂	b ₁	0	1	0	1	0	1	0	1	0	1	0	1	0	1
C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N		C O L U M N	
R O W		R O W		R O W		R O W		R O W		R O W		R O W		R O W		R O W		R O W	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	NUL	DLE	1	1	2	3	4	5	6	7	8	9	0	1
0	0	0	0	0	1	SOH	DC1	LLO	1	A	Q	P	a	1	1	1	1	1	1
0	0	0	1	0	2	STX	DC2	1	1	B	R	b	2	1	1	1	1	1	1
0	0	1	1	3	ETX	1	1	1	1	C	S	c	3	1	1	1	1	1	1
0	1	0	0	4	EOT	SDC	DC4	DCL	5	D	T	d	4	1	1	1	1	1	1
0	1	0	1	5	ENQ	PPC	NAK	PPU	6	E	U	e	5	1	1	1	1	1	1
0	1	1	0	6	ACK	1	1	1	1	F	V	f	6	1	1	1	1	1	1
0	1	1	1	7	BEL	1	1	1	1	G	W	g	7	1	1	1	1	1	1
1	0	0	0	8	BS	GET	CAN	SPE	1	H	X	h	8	1	1	1	1	1	1
1	0	0	1	9	HT	TCT	EM	SPD	1	I	Y	i	9	1	1	1	1	1	1
1	0	1	0	10	LF	1	1	1	1	J	Z	j	10	1	1	1	1	1	1
1	0	1	1	11	VT	1	1	1	1	K	{	k	11	1	1	1	1	1	1
1	1	0	0	12	FF	1	1	1	1	L		l	12	1	1	1	1	1	1
1	1	0	1	13	CR	1	1	1	1	M	~	m	13	1	1	1	1	1	1
1	1	1	0	14	SO	1	1	1	1	N	^	n	14	1	1	1	1	1	1
1	1	1	1	15	SI	1	1	1	1	O	_	o	15	1	1	1	1	1	1

ADDRESSED COMMAND GROUP (ACG) UNIVERSAL COMMAND GROUP (UCG) LISTEN ADDRESS GROUP (LAG) TALK ADDRESS GROUP (TAG) SECONDARY COMMAND GROUP (SCG)

PRIMARY COMMAND GROUP (PCG)

- NOTES:
- ① MSG = INTERFACE MESSAGE
 - ② b₁ = DIO1...b₇ = DIO7
 - ③ REQUIRES SECONDARY COMMAND
 - ④ DENSE SUBSET (COLUMN 2 THROUGH 5). ALL CHARACTERS USED IN BOTH COMMAND & DATA MODES.